Integrated impedance bridge for capacitance measurements at cryogenic temperatures and finite magnetic fields.

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Roll No: MS16054

*A dissertation submitted for the partial fulfilment
of BS-MS dual degree in Science*
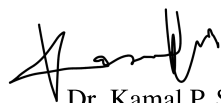
Under the guidance of

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Indian Institute of Science Education and Research Mohali

May 2021

Certificate of Examination

This is to certify that the dissertation titled **Integrated impedance bridge for absolute capacitance measurements at cryogenic temperatures and finite magnetic fields.** submitted by **Abhishek Purohit** (Reg. No. MS16054) for the partial fulfillment of BS-MS dual degree programme of the Institute, has been examined by the thesis committee duly appointed by the Institute. The committee finds the work done by the candidate satisfactory and recommends that the report be accepted.

Dr. Kamal P. Singh   Dr. Satyajit Jena   Dr. Ananth Venkatesan

(Supervisor)

Dated: 01.05.2021

Declaration

The work presented in this dissertation has been carried out by me under the guidance of Dr. Ananth Venkatesan at the Indian Institute of Science Education and Research Mohali.

This work has not been submitted in part or in full for a degree, a diploma, or a fellowship to any other university or institute. Whenever contributions of others are involved, every effort is made to indicate this clearly, with due acknowledgement of collaborative research and discussions. This thesis is a bonafide record of original work done by me and all sources listed within have been detailed in the bibliography.

<div align="right">

Abhishek Purohit

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In my capacity as the supervisor of the candidate's project work, I certify that the above statements by the candidate are true to the best of my knowledge.

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Dr. Ananth Venkatesan

(Supervisor)

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Abstract

Nanoscience has been an evolving and rapidly expanding discipline in the last decade. This includes both recent work and more advanced ideas. Nanomaterials, nanodevices, and nanomeasurement and nanocharacterization are three major areas of nanoscience and nanotechnology. As system scaling continues in nanometer scale and new nanodevices emerge, accurate characterization and detailed understanding of their electronic structure becomes increasingly important, yet difficult. Technological advancements over the years, have empowered us today to measure capacitance precisely. But a need to further improve to measurement of small capacitance changes is required as the ongoing miniaturisation of the electromechanical devices pushes the measurement techniques to the limit.

In this work we have designed a set-up for high precision capacitance measurements at low temperatures and high magnetic fields. In the first chapter we talk about current capacitance measurement devices used and need for an improvement. In second chapter we discuss some key concepts of making and working principles of capacitance measuring instruments and moving on in the third chapter we have described the experimental set-up and discussed thoroughly about all the components used and fabricated. And in the final chapter talks about the progress we have made so far in fabricating the components, results so far and future work.

Chapter 1

Introduction

The functionality of electronic and electromechanical devices is defined by their impedance. As a result, an effective impedance measurement method is important for designing, characterising, and optimising electronic and electromechanical devices. An accurate measurement of the capacitance is very necessary as we start exploring exploring the electronic structures of various nanostructures.

We are able to measure capacitance precisely due to advancements in technology.But a need to further improve to measurement of small capacitance changes is required as the ongoing miniaturisation of the electromechanical devices pushes the measurement techniques to the limit.[ITRS]

In this chapter we discuss concepts essential for subsequent discussions and give a basic outline for the need of using such set-ups for measuring capacitance.

1.1 Density of states

The density of states (DOS) essentially indicates the number of different states at a particular energy level which can be occupied by electrons, i.e. the number of electron states per unit volume per unit energy. Determining the DOS of a material is essential as bulk properties like specific heat, paramagnetic susceptibility, and other transport properties of conductors depend on this function [Ben Mahmoud 20].Waves, or wave-like particles, can occupy modes or states in quantum mechanical systems, with wavelengths and propagation directions determined by the system. For example, the interatomic spacing and atomic charge of a material may allow only electrons of specific wavelengths to exist in some sys-

tems.Only certain states are often allowed. As a result, it's possible that many states are eligible for occupation at one energy level and none are available at another.

When considering the density of states of electrons at the band edge between the valence and conduction bands in a semiconductor, an increase in electron energy allows more states available for occupation for an electron in the conduction band. Alternatively, if the density of states is discontinuous for a given energy interval, no states are accessible for electrons to occupy within the material's band gap. In order to transition to a different state in the valence band, an electron at the conduction band edge must sacrifice at least the band gap energy of the material.This dictates whether the material is an insulator or a metal in the propagation dimension. The number of states in a band can also be used to predict conduction properties.The topological properties of the system such as the band structure, have a major impact on the properties of the density of states.

1.2   Quantum Capacitance

The concept of "quantum capacitance" was used by Luryi in order to develop an equivalent circuit model for devices that incorporate a highly conducting two-dimensional (2D) electron gas. Recently, this term has also been used in the modeling of one-dimensional (1D) systems, such as carbon nanotube (CN) devices.Quantum capacitance is particularly important for low-density-of-states systems, such as a two-dimensional electronic device on a semiconductor surface or interface, or graphene [Cheremisin 15], and can be used to construct an experimental energy functional of electron density.

In such systems with a low density of states, the total capacitance needs to be expressed by the quantum capacitance C_q in series to the geometric capacitance C_g leading to a total capacitance C_{tot} :

$$\frac{1}{C_{tot}} = \frac{1}{C_g} + \frac{1}{C_q} \tag{1.1}$$

$$C_{tot} = \frac{C_q C_g}{C_q + C_g} \tag{1.2}$$

which is also strongly depending on the density of states. A dielectric layer separates the channel from the gate electrode in most field-effect semiconductor devices. The capacitance measured at the gate is the amount of the geometric capacitance associated with the

dielectric, C_g, and the capacitance associated with adding carriers to the semiconductor's bandstructure, or quantum capacitance, C_q which is DOS dependent.Quantum capacitance can be relevant in capacitance–voltage profiling.

1.3 Current capacitance measuring tools

A **capacitance meter** is a piece of electronic test equipment that is used to calculate the capacitance of discrete capacitors. The capacitance may be shown only, or the metre may also calculate leakage, equivalent series resistance (ESR), and inductance, depending on the sophistication of the metre.The capacitor must be removed from the circuit for most purposes and in most cases; ESR can typically be calculated in circuit.

Figure 1.1: Capacitance meter.

A **LCR meter** is a piece of electronic test equipment that measures an electronic component's inductance (L), capacitance (C), and resistance (R).An LCR meter is suitable for measuring inductors, capacitors, and resistors directly and precisely at various test frequencies. The test area can be manually or automatically picked.Wheatstone bridge and RC ratio arm circuits are important parts of an LCR meter. One of the bridge's arms is linked to

the part whose value is to be calculated. Similar provisions apply to various types of measurements.The bridge is adjusted in null position in order to balance it completely. Besides, the sensitivity of the meter should also be adjusted along with balancing of the bridge. The output from the bridge is fed to emitter follower circuit. The output from emitter follower circuit is given as an input to detector amplifier.

Figure 1.2: Benchtop LCR meter with 4-wire (Kelvin sensing) fixture.

Capacitance measurements are usually done using bridge circuits(discussued in chapter 2) and LCR meters. Andeen-Hagerling model 2700A precision capacitance and loss measurement bridge is one of the highest resolution CV meter commercially available.The AH 2700A offers unparalleled stability, resolution, linearity and accuracy in a multi-frequency capacitance/loss bridge (whether manual or automatic) [Cap]. Its numerous state-of-the-art features make it an exceptionally user-friendly instrument. The precision of the AH 2700A is creating new applications in calibration, science, and production in a wide range of fields. The AH2700A measures capacitance and loss in medium- and high-impedance ranges, and thus allows using three-terminal rather than five-terminal connections to the DUT (Device Under Test). Its unmatched precision is the result of a uniquely designed

Figure 1.3: Andeen-Hagerling model 2700A

ratio transformer which is the culmination of over 40 years of bridge design and manu-facture. Equally important is the unique temperature-controlled, fused-silica capacitance standard which allows extremely high measurement stability and immunity to mechanical shock. These elements combine to form a true bridge operating at 50 Hz - 20 kHz to give capacitance/loss results which are independent of the exact test frequency.The commercial bridge's output was first measured using a typical shielded 9.3pF capacitor. The mea-sured sensitivity is, as predicted, a strong feature of the test signal (200 and 80 aF/$\sqrt{Hz}$ for 100mV and 250mV rms test signals, respectively, in good agreement with the manufacturer specification). We intend to surpass its precision with our instrument.

1.4 Need for improvement in capacitance measurements.

With the ongoing miniaturisation of nanomechanical devices when the density of available electronic states in nanostructures becomes finite which results in a so-called quantum ca-pacitance or the displacement of electromechanical devices enters the nanoscale.In such nanoscale devices, a low DOS can reduce the quantum capacitance to hundreds of atto-farads, making C_q dominate the total capacitance.Typically while measurement of such systems, capacitance changes only by a few attofarads.However, bridge circuits and LCR meters usually include some lengthy cables which give rise to a parasitic capacitance in the order of hundreds of picofarads.Because of the high parasitic capacitance, the probe signal

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is greatly attenuated, which, when combined with the necessary excitation, drives attofarad capacitance changes below the resolution limit.To reduce the effect of the parasitic capacitance of the cables **Hazegi** [Hazeghi 11] used a high-electron mobility transistor (HEMT) as an impedance-matching amplifier in an integrated capacitance bridge. We develop our intrument based on it.

Chapter 2

Capacitance Bridge and FETs

The core of our setup consists of a capacitance bridge and an impedance matching amplifier. The amplifier consists of a HEMT (High Electron Mobility Transistor) which is a type of FET (Field Effective Transistor). In this chapter we discuss in detail about these two essential components and related principles

2.1 Working of capacitance bridges

The capacitance of an unknown capacitor is calculated against a standard reference in a capacitance bridge.The voltage V induced at the "centre point" of the bridge is given by the following equation for a voltage V_s applied to the sample capacitor and a voltage V_r applied to the reference capacitor. [Steele]

$$C_T V = C_s V_s + C_r V_r \tag{2.1}$$

where C is the total capacitance at the bridge's centre point and is equal to

$$C_T = C_s + C_r + C_g \tag{2.2}$$

where the cumulative stray capacitance to ground is denoted by Cg.Choosing an appropriate voltage V_r of the opposite sign (or 180 degrees out of phase for an AC signal) to V_s and of a magnitude such that the voltage V at the centre of the bridge is nulled allows us a precise measurement of the value of the sample capacitance.The capacitance bridge has the advantage of allowing an accurate measurement of the sample capacitance without the need for a separate measurement of the shunt capacitance or the gain of any amplifiers used to measure V.
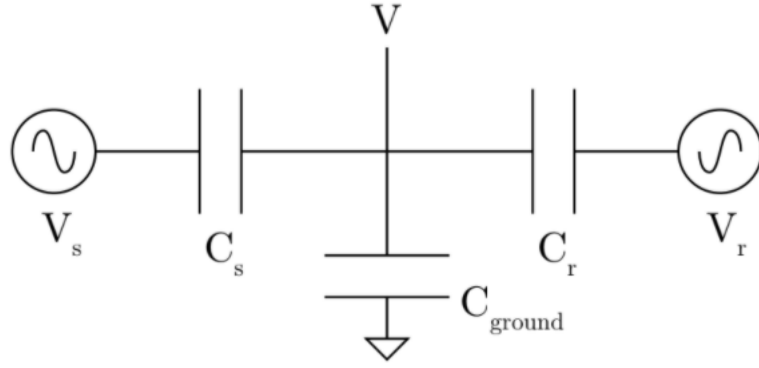
Figure 2.1: Capacitance bridge schematic diagram. To balance the bridge we adjust the amplitude and phase of V_r such that we get null voltage V at the bridge point.

The sample capacitance is calculated by balancing the bridge in this way is given by:

$$C_s = \frac{C_r V_r}{V_s} \tag{2.3}$$

Small variations in sample capacitance in response to changes in experimental parameters such as bias voltage or magnetic field are of particular interest to us. These changes are very small, often in attofarad units compared to the the sample capacitance.We don't balance the bridge at each point for these measurements; instead, we use the bridge to null the broad background signal.We now gain a major technological advantage here because we are now measuring small changes in a small signal rather than large changes in a large signal.The shift in sample capacitance is directly related to the remaining out of balance signal we measure.

If we assume these changes ΔC_s small compared to the total capacitance C_T we get

$$C_T(V + \Delta V) = (C_s + \Delta C_s)V_s + C_r V_r \tag{2.4}$$

If the bridge was balanced at the start, the out of balance signal becomes:

$$\Delta V = \frac{V_s}{C_T}\Delta C_s \tag{2.5}$$

This enables us to turn out of balance voltage readings into changes in sample capacitance directly.

This also highlights a significant aspect of the capacitance bridge technique: as seen in the above expression, the capacitance bridge's out of balance signal is inversely proportional to the total capacitance at the bridge's centre. In order to maximize the sensitivity of the bridge, the stray capacitance to ground C_g should be minimized.Using a room temperature amplifier to measure the voltage while operating with a fF sample capacitance will result in substantial signal loss since the cables running to the top of the cryostat have a shunt capacitance of at least 200 pF, hence we require a cryogenic amplifier to serve this purpose. Now if if we are measuring an unknown impedance Y_{DUT} with the output from the bridge going to a transistor which acts as an impedance matching amplifier[Verbiest 19]. The signal vb at the bridge point is an average of the applied AC signals v_{ref} and v_{DUT},

$$v_b = \frac{Y_{DUT}.v_{DUT} + Y_{ref}.v_{ref}}{Y_{ref} + Y_{DUT} + Y_{par}} \tag{2.6}$$

and when the bridge is balanced Y_{DUT} is given by

$$Y_{DUT} = -\frac{Y_{ref}.v_{ref}}{v_{DUT}} \tag{2.7}$$

We only need to characterise the other admittances in the circuit once because Y_{DUT} is the only quantity that is tunable with the DC voltage V_{DUT}. The HEMT amplifies the signal v_b AHEMT times to produce the output voltage $v_{out} = A_{HEMT}.v_b$, which is measured with a lock-in amplifier where A_{HEMT} is the amplification. The sensitivity S of the circuit to a change in Y_{DUT} is given by

$$S = \frac{Y_{ref}.(v_{DUT} - v_{ref}) + Y_{par}.v_{DUT}}{(Y_{ref} + Y_{DUT} + Y_{par})^2} \tag{2.8}$$

Assuming Y_{DUT} is a pure capacitor, the smallest detectable change δC_{DUT} in C_{DUT} is given by

$$\delta C_{DUT} = \frac{v_{noise}}{A_{HEMT}.S} \tag{2.9}$$

v_{noise} is the spectral density of the voltage noise arriving at the lock-in amplifier's input stage, which is 2π times the measurement frequency. For our experiment we intend to calibrate our set-up using varactor diode as DUT and do a complete noise characterisation. Our entire set-up works on the above mentioned principle of capacitance bridge with an impedance matching amplifier.

2.2 Microstrip

Microstrip line is used to carry Electro-Magnetic Waves (EM waves) or microwave frequency signals. It consists of 3 layers, conducting strip, dielectric and Ground plane [Pozar]. It is used to design and fabricate RF and microwave components such as directional coupler, power divider/combiner, filter, antenna, MMIC etc. A microstrip line constitutes of a conductor of width W, a dielectric substrate of thickness d and permittivity ϵ_r. The presence of the dielectric (commonly thin with d $<< \lambda$) concentrates the field lines in the region between the between the conductor and the ground [Maurya] plane, with some fraction being in the air region above the conductor, leading to quasi-TEM modes of propagation in which dispersion occurs as a function of wavelength.
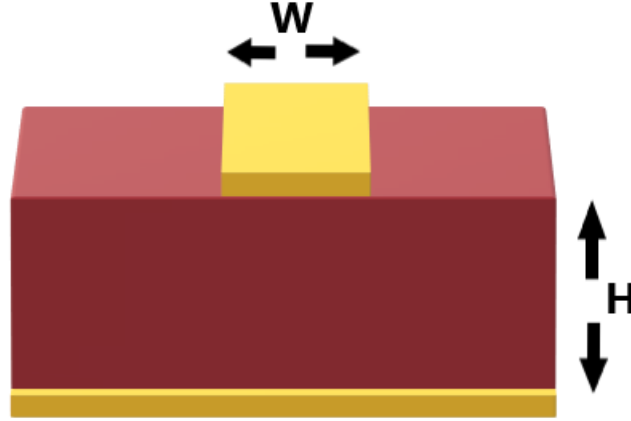

Figure 2.2: Microstrip.

$$\text{If } \left(\tfrac{W}{H}\right) < 1:$$
$$\varepsilon_{eff} = \tfrac{\varepsilon_R+1}{2} + \tfrac{\varepsilon_R-1}{2}\left[\frac{1}{\sqrt{1+12\left(\frac{H}{W}\right)}} + 0.04\left(1-\left(\tfrac{W}{H}\right)\right)^2\right]$$
$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}}\ln\left(8\left(\tfrac{H}{W}\right) + 0.25\left(\tfrac{W}{H}\right)\right) \tag{2.10}$$
$$\text{If } \left(\tfrac{W}{H}\right) > 1:$$
$$\varepsilon_{eff} = \tfrac{\varepsilon_R+1}{2} + \left[\frac{\varepsilon_R-1}{2\sqrt{1+12\left(\frac{H}{W}\right)}}\right]; Z_0 = \frac{120\pi}{\sqrt{\varepsilon_{eff}}\left[\frac{W}{H}+1.393+\frac{2}{3}\ln\left(\frac{W}{H}+1.444\right)\right]}$$

Microstrip line will have low to high radiation, will support 20 to 120 ohm impedance, supports Q factor of about 250. The RF/microwave product made using microstrip line is less expensive and lighter in weight compare to its waveguide counterpart. Usually FR-4 dielectric substrate is used as PCB for microstrip based etching due to its low cost.

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2.3 Field Effective Transitors (FET) and HEMTs

The field-effect transistor (FET) is a type of transistor that controls current flow using an electric field. FETs are three-terminal devices with a source, gate, and drain. The application of a voltage to the gate, which alters the conductivity between the drain and source, controls the flow of current in FETs. The control electrode called the gate is placed in very close proximity to the channel so that its electric charge is able to affect the channel. HEMTs are field effect transistors in which a third contact, the gate, controls the current
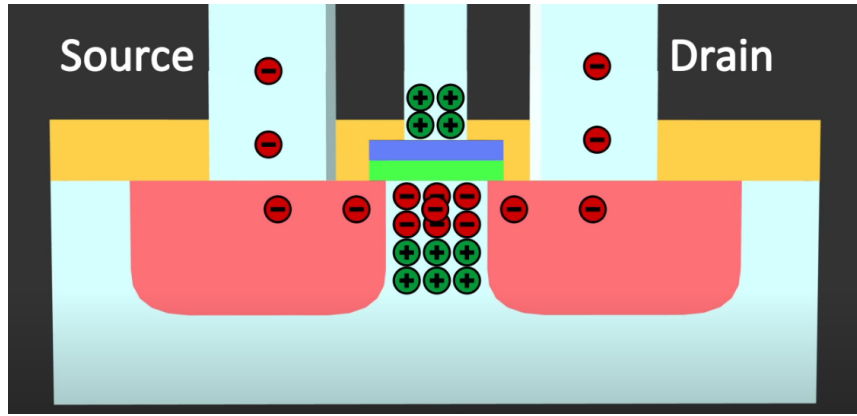

Figure 2.3: Working of FETs

flow between two ohmic contacts, the source and drain. The gate is usually a Schottky contact. HEMTs, unlike ion implanted MESFETs, are made up of epitaxially grown layers with varying band gaps E_g. Electrons are transferred from the material with the higher conduction band energy E_c to the material with the lower E_c in the vicinity of a semiconductor heterojunction, where they can occupy a lower energy state. This can be a significant number of electrons, particularly if the semiconductor has a high E_c barrier. A two-dimensional electron gas (2DEG), or channel, is formed near the interface. This allows the electrons in the channel to be separated from their donor atoms, reducing Coulomb scattering and thereby increasing the mobility of the conducting electrons. When a channel is formed with just a single heterojunction, electrons easily penetrate the buffer beneath the channel, where their mobility is normally lower and gate control is weak. A second energy barrier below the channel may be added by a material with a higher EC than the channel material to hold the electrons in the channel.

The specialised PN junction that a HEMT employs is its most important component. It's called a hetero-junction, and it's made up of two junctions with different materials on each

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side. Aluminium gallium arsenide (AlGaAs) and gallium arsenide were the most commonly used components (GaAs). Gallium arsenide is commonly used because it has a high degree of basic electron mobility, which is important for the device's operation. Since silicon has a much lower degree of electron mobility, it is not used.The doped layer of aluminium gallium arsenide about 500 Angstroms thick is set down above this. The gate is generally made from titanium, and it forms a minute reverse biased junction similar to that of the GaAsFET. Many electrons from the n-type region remain close to the hetero-junction as they pass through the crystal lattice. These electrons form a one-electrons-thick film, which is referred to as a two-dimensional electron gas [Aadit]. Since there are no other donor electrons or other objects with which electrons can collide within this field, electrons can move freely, and the mobility of electrons in the gas is very high. The number of electrons in the channel formed from the 2 D electron gas is modulated by a bias applied to the gate formed as a Schottky barrier diode, which governs the device's conductivity. As compared to more common forms of FETs, where the channel width is regulated by the gate bias, this is a significant improvement. HEMTs are widely used because of their high speed and low
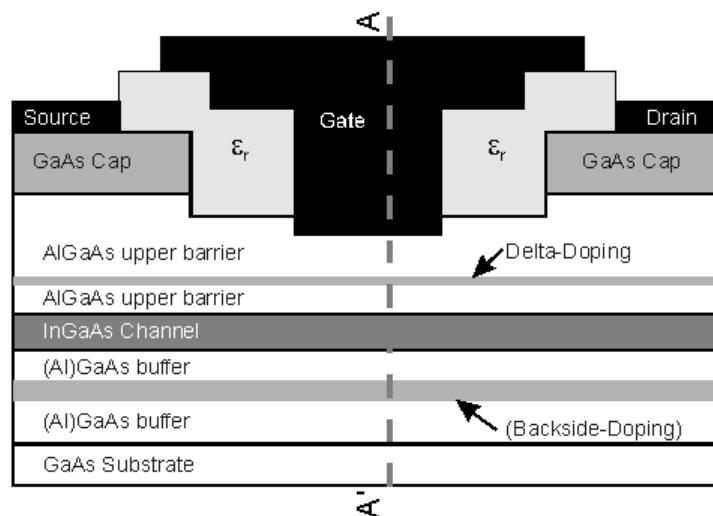

Figure 2.4: Schematic cross section of a High Electron Mobility Transistor (HEMT).

noise figure. This is related to the nature of the two dimensional electron gas and the fact that there are less electron collisions. They are commonly used in low noise small signal amplifiers, power amplifiers, oscillators, and mixers operating at frequencies up to 60 GHz and beyond due to their noise efficiency and we have used them as cryogenic amplifiers.

Chapter 3

Experimental Setup

In this work, we make the previously reported integrated capacitance bridge into an integrated impedance bridge to determine the absolute capacitance by taking inspiration from the setup of **G. J. Verbiest**. We also design the circuit in such a way that future plans of doing magnetic field-dependent measurements would also be possible.
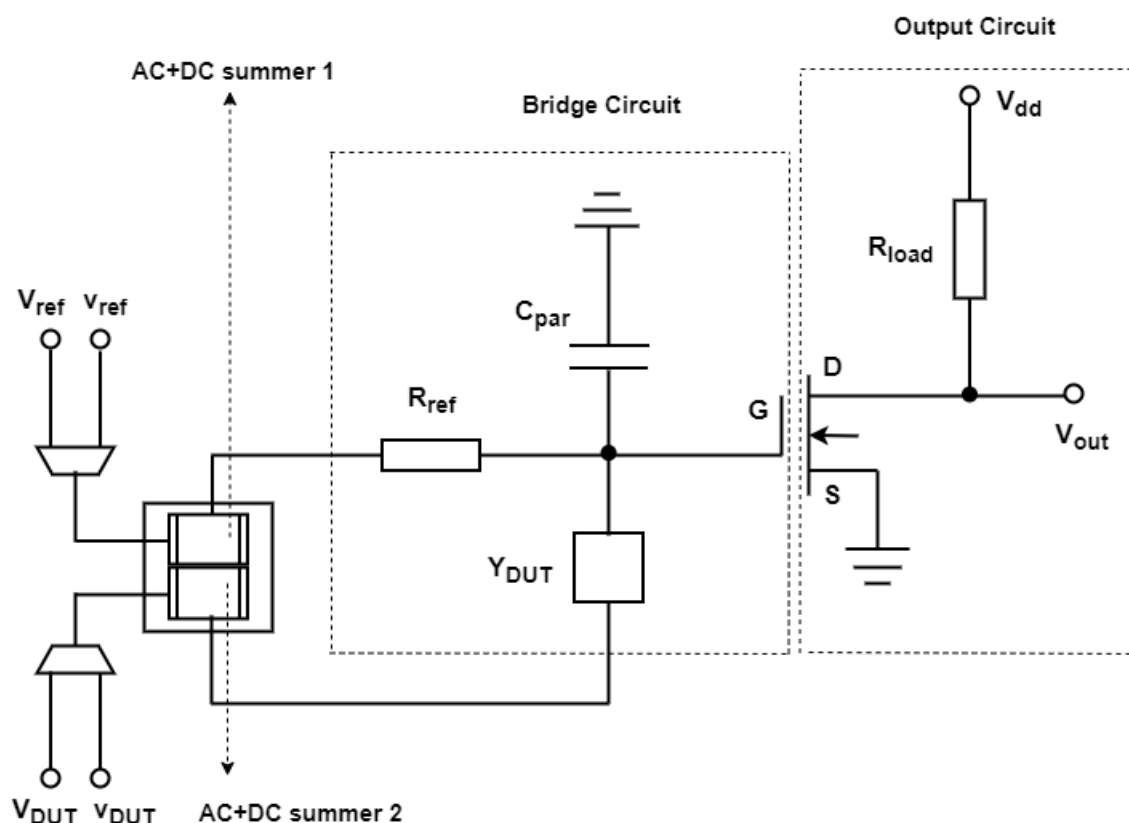

Figure 3.1: Schematic of the capacitance bridge setup.The circuit consists of input ports , a bridge circuit and an output circuit.

The design of the measurement circuit, which consists of a bridge circuit and an output circuit that are coupled via a HEMT amplifier. The bridge circuit contains a reference resistor of 1 MΩ, a parasitic capacitance C_{par} to ground, and an unknown admittance Y_{DUT}. The output circuit has a load resistor of 1 kΩ and an output line for V_{out}. We have fabricated the bridge circuit and output circuit on separate PCBs so that we can attach the output circuit containing the HEMT perpendicular to the bridge circuit in future to do magnetic field dependent measurements.
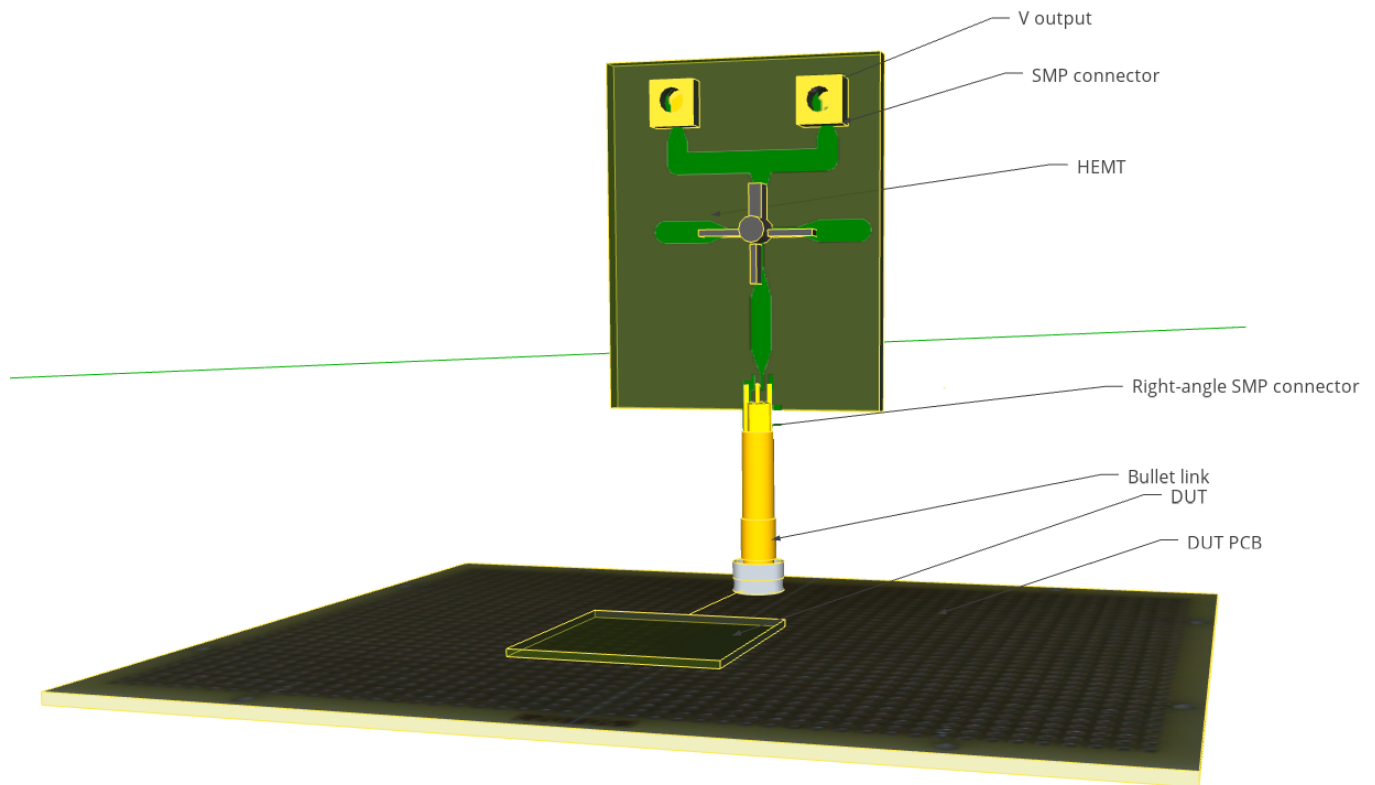

Figure 3.2: CAD diagram of the capacitance bridge setup. We place the output circuit perpendicular to the DUT PCB in order to perform future magnetic field dependent measurements.

To reduce the output circuit's heat load, we always place R_{load} to room temperature (RT) and not on the output PCB containing the HEMT. In this chapter we will discuss about the specifications of each component of the setup and why they were chosen.

3.1 AC+DC summer/adder

Our experiment involves AC and DC measurements.We require adjustable AC signals of wide range of frequencies for the working of our bridge circuit as explained in chapter 2. But along with it we also require to give DC voltages to bias the active component of our circuit ie. the HEMT(High Electron Mobility Transistor). We aslo require another source of DC bias for the varactor diode to test the working of our measurement device.

There are various ways to add AC and DC signals. The most widely used devices are bias tees.A Bias tee is a three-port device.The bias tee can be thought of as a combination of an ideal capacitor that allows AC but blocks DC bias and an ideal inductor that blocks AC but allows DC. While some bias tees can be produced with only an inductor and a capacitor, wideband bias tees are far more difficult to construct due to parasitic elements in practical components.
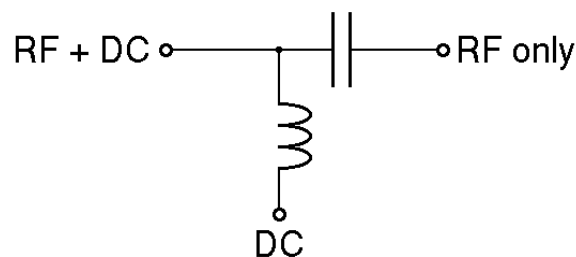

Figure 3.3: Equivalent circuit of a bias tee

For our experiment we decided to take inspiration from **Arash Hazeghi** who used an audio transformer to make to add AC and DC and build our own circuit for the same.AC and DC signals are added together with the help of Triad Magnetics SP-67 audio transformer.
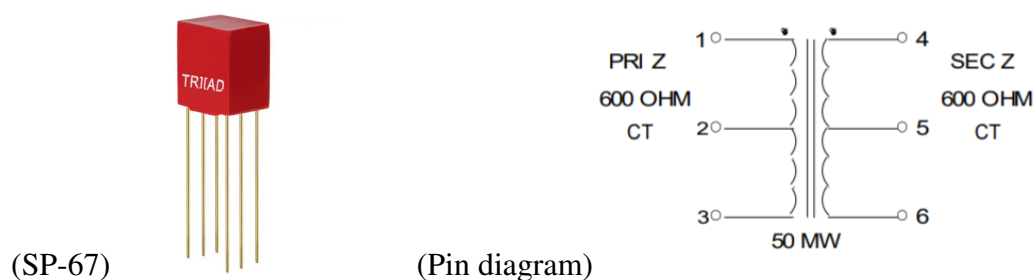

Figure 3.4: Triad Magnetics SP-67 audio transformer

Since we were in need of two AC and DC signal adding ports, we decided to place both of them on a single PCB and solder the connections. This PCB takes AC and DC inputs from constant sources and feeds the added signal into our bridge circuit and the transistor.
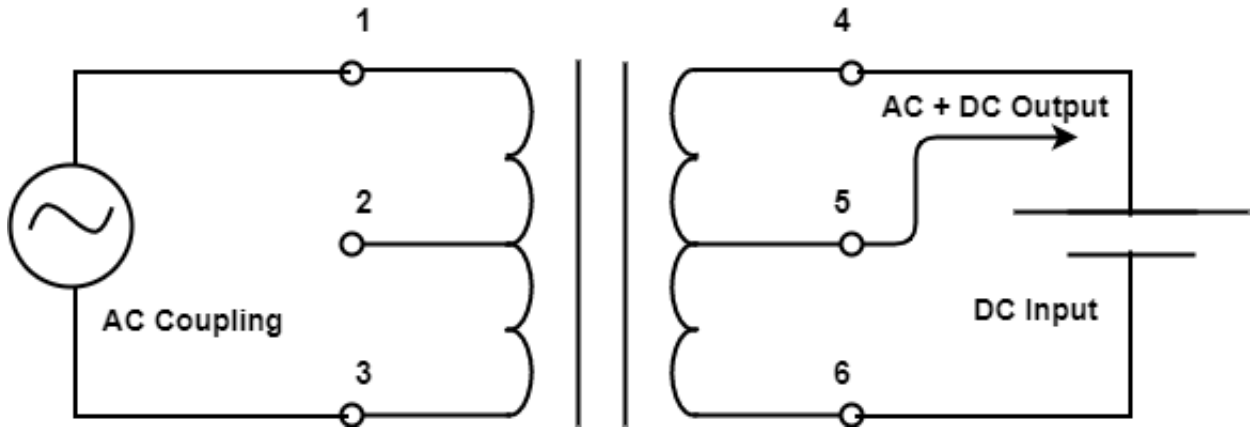

Figure 3.5: Circuit diagram of the AC+DC summer circuit

We make the connections to SP67 as per the above diagram. We give AC input across pin 1 and 3, DC input across pin 4 and 6 and take AC + DC output from pin 5. We make two such circuits on a single PCB; one to the DUT (Device Under Test) and one to the reference resistor. We also make a common ground point in our circuit. The result showing the addition AC and DC signals of our input circuit is shown in Chapter 4.
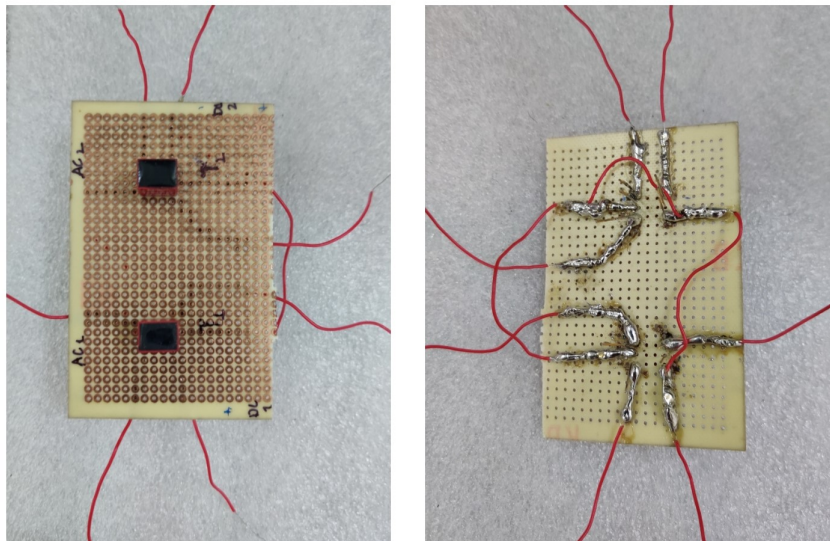

Figure 3.6: Front and back view of the soldered AC+DC summer PCB. The PCB contains 2 such circuits.

3.2 Bias controller

A voltage regulator is a device that maintains a steady voltage automatically. Negative feedback or a basic feed-forward configuration may be used in a voltage regulator. An electromechanical device or electronic components may also be used. Although for the final experiment we have used commercially produced constant DC voltage voltage sources. For testing purposes throughout our experiment we designed a voltage regulator circuit that takes input from a 9V batteru and steps it down and provides constant DC voltage as per our requirement. It mainly consists of a potentiometer, a rseistor and a LM 317 IC. The LM-317 is readily available integrated circuit that works as a voltage regulator.
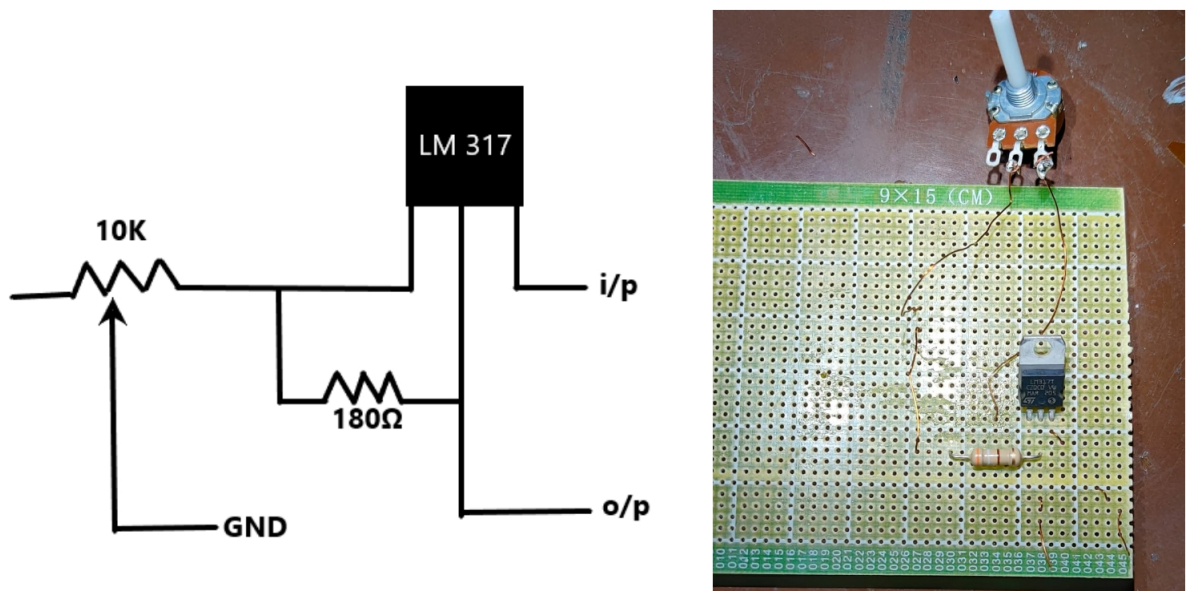

Figure 3.7: Circuit diagram and soldered circuit of the bias controller made using LM-317.

3.3 Bridge Circuit

The bridge is made up of a reference impedance and an impedance-matching amplifier that drives the huge parasitic cable capacitance and isolates the system under examination (DUT). We use a GaAs-based high electron mobility transistor (HEMT) as the impedance-matching amplifier since we are interested in measurements over a broad temperature range,

down to cryogenic temperatures. The bridge circuit is made on a separate PCB to carry out future magnetic field dependent measurements. The DUT PCB was made using photo-lithography technique which was also optimised.
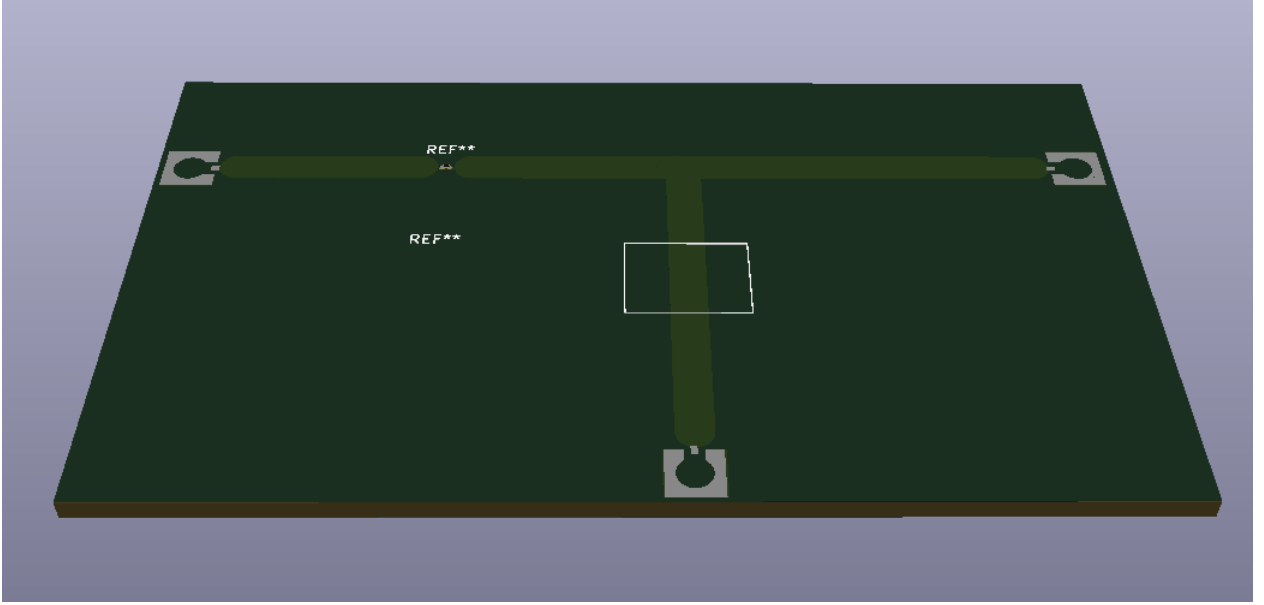

Figure 3.8: KiCad design of the DUT PCB

3.3.1 Reference Resistor

The choice of the reference resistor is very crucial for the working of the set-up. There are various things we need to keep in mind while choosing the R_{ref}. The reference impedance is used to balance the signal through the DUT, and its AC impedance must be greater than the HEMT gate AC impedance to prevent the DUT signal from shunting. R_{ref} should be much smaller than the HEMT DC gate resistance across all temperatures since the HEMT gate (G) is biased by R_{ref}. R_{ref} also serves as a low-pass filter when combined with C_{par} and Z_{DUT}'s capacitive contribution. To avoid additional shunting of the signal across Z_{DUT}, we select R_{ref} equal to the predicted Z_{DUT} impedance parallel to a parasitic capacitance C_{par} at the measurement frequency. We use a 500 MΩ reference resistance R_{ref} with a low temperature coefficient to satisfy these constraints and maximise bandwidth (SMD type thick film resistor).

3.3.2 Device Under Test (DUT)

This set-up can be used to measure capacitance and change in capacitance for various samples. The samples we would be using are DUTs. We need to use a voltage operated capacitor (SMV1249-079LF) as the DUT to optimise the resolution for determining Y_{DUT}. These tests have to be carried out at room temperature. All of the measurements in this experiment are going to be done at a frequency of 100 kHz. DC sources were used to apply the necessary bias potentials. A lock-in amplifier is used to measure the output of the bridge circuit SMV1249-079LF is a type of varactor diode whose capacitance changes with the change in bias voltages.We can change the bias voltages and find the capacitance for various applied biases and compare them with its data-sheet to confirm the working of the set-up. After we use a varactor diode to confirm the working of our setup we
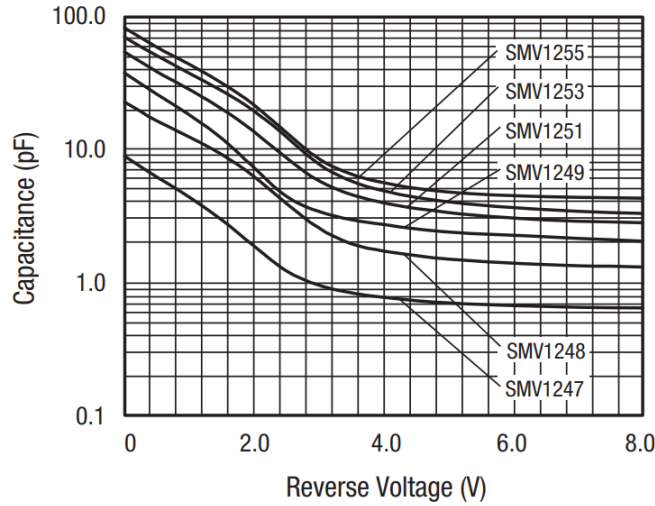

Figure 3.9: Capacitance vs reverse voltage of SMV1249-079LF

can use various samples to measure their capacitance. Direct measurements of the density of states via the quantum capacitance have been successful for among others, graphene and carbon nanotube devices as well as GaAs-based devices containing a two-dimensional (2D) electron gas. For future experiments we plan on putting a graphene sample as DUT. Graphene exhibits an electronic band structure, where the conduction band and the valence band touch in (two) so called Dirac points. The energy-momentum relation is linear around each Dirac point which directly results in a linearly varying density of states and thus a quantum capacitance C_q that linearly varies with the Fermi energy.

3.3.3   Microstrip fabrication using photo-lithography

A Microstrip is a type of electrical transmission line used to transmit RF signals and are commonly fabricated using printed circuit board (PCB) technology as discussed earlier. All signals in the circuit are sent via microstrips in this set-up hence it is crucial for us to fabricate these strips of caluculated width to get our required impedance as accurately as possible. The mictrostrips of 3mm width for the DUT PCB were fabricated using the photo-lithography technique.
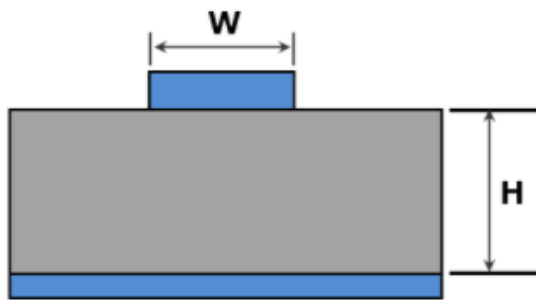
Result:
Width/Height: 1.875
Effective Dielectric Constant: 3.325
Impedance: 50.83 Ω

Figure 3.10: Mictrostrip schematic   Figure 3.11: Microstrip calculator

Photolithography is a microfabrication technique for patterning sections on thin films or the bulk of a substrate (also called a wafer). A geometric pattern is transferred from a photomask (also known as an optical mask) to a photosensitive chemical photoresist on the substrate using light. Following that, a series of chemical treatments either etches the exposure pattern into the substrate or allows for the deposition of a new material in the desired pattern onto the material underneath the photoresist.[Stevenson] Cleaning the substrate (FR4 PCB inour case) to remove any dirt/contaminates, dehydrating the substrate to remove any water, and then adding an adhesion promoter are important first step. Once the substrate has been prepared the photoresist can be applied to the surface.The resist-covered substrate is then aligned to the photomask and exposed to UV light as the next step in the photolithography process. The solubility of the photoresist changes after it is exposed to UV light, which is a crucial concept in photolithography. The form of photoresist – positive or negative – and the details of the production process that should be used are determined by how this solubility varies.There are two types of photoresists: positive and negative. The portion of the film that is exposed to the resist becomes more soluble and can be dissolved with a developer in a positive resist. In a negative, where the resist has been exposed to light, the resist becomes stronger and the creator is unable to remove it. We used nega-

tive photoresists for all our PCBs. Resist comes in a variety of compositions and versions, allowing for the creation of various heights, temperatures, exposure conditions, and structures. Now we carefully paste the designed photomask we designed using KiCad on the photoresist and align it carefully. We then place our PCB inside a UV box and expose the photomask side to the UV lamp.
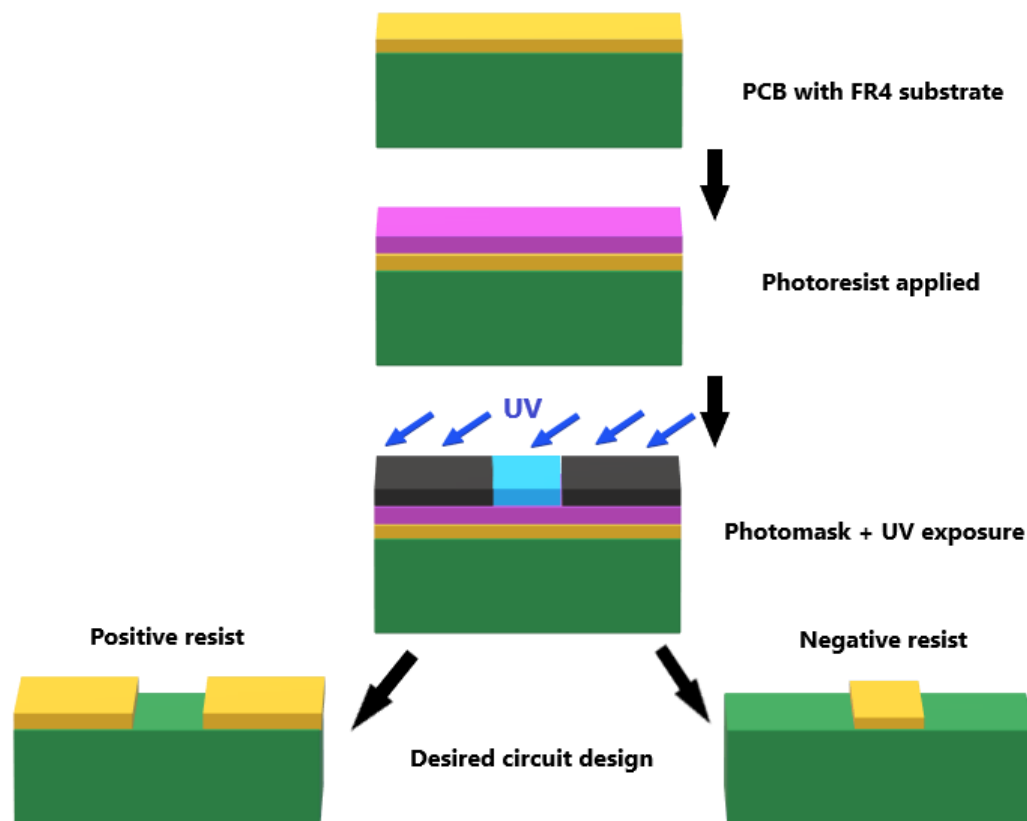

Figure 3.12: Steps for photolithography.

The final step is developing the PCB by etching it with various chemicals for various durations which we have optimised as seen in the table below.

Photolithography Optimisation		
Exposure/ Chemical	Conc. (g/ml)	Time (s)
UV	–	40
Na_2CO_3	3/100	10
NaOH	2/50	40
$FeCl_3$	8/50	1800

3.4 Output Circuit

The output circuit consists of a load resistor R_{load} and the drain (D) to source (S) resistance of the HEMT. It acts as an impedance matching amplifier the output of which is collected using a lock-in amplifier. Again this is made on a separate PCB for future magnetic field dependent experiments in which the output circuit will be placed perpendicular to the bridge circuit PCB and parallel to the magnetic field. The design of the output circuit was made using KiCad and the the circuit was printed commercially from its gerber files for higher precision.
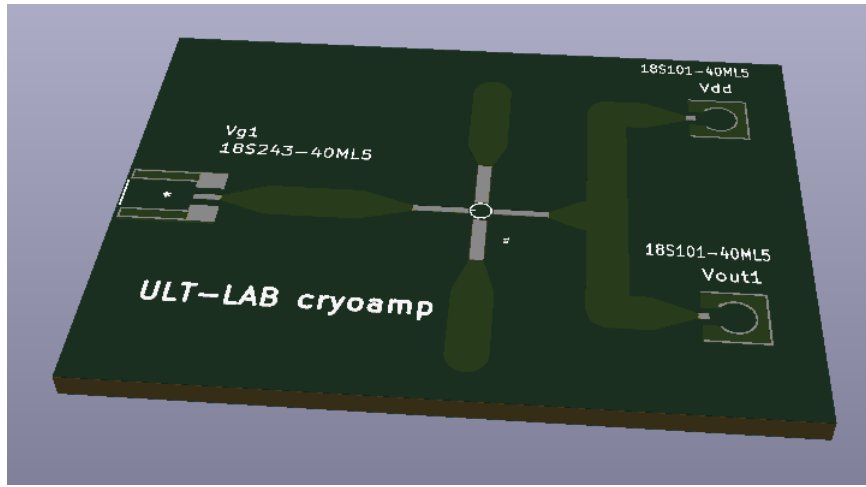

Figure 3.13: Steps for photolithography.

3.4.1 High Electron Mobility Transistor (HEMT)

A high-electron-mobility transistor (HEMT), also known as a heterostructure FET (HFET) or a modulation-doped FET (MODFET), is a field-effect transistor that uses a heterojunction (i.e., a heterojunction) as the channel rather than a doped area. The advantage of using HEMTS is fast switching speeds are achieved because the main charge carriers in MODFETs are majority carriers, and minority carriers are not substantially involved; and exceptionally low noise values are achieved because the current variance in these devices is low relative to other devices. We use a (GaAs-based) HEMT as an impedance-matching amplifier to ensure the bridge's functionality down to cryogenic temperatures. For our set-up we decided to go with Mitshibushi GaAs FET MGF1302 for its low noise figure and high gain. [Mitsubishi]

Model	D-S Vol	Frequency Range	Low noise figure	High Gain	Bias I
MGF1302	3 V	1 to 12 GHz	1.4 dB @ 4 GHz	11.0 dB @ 4GHz	10 mA

Table 3.1: HEMT specifications.

The packaging is a ceramic microstrip (SMT) packaging. The HEMT is the only active component of the output circuit. A standard Si FET is unsuitable due to carrier freeze-out at low temperature.
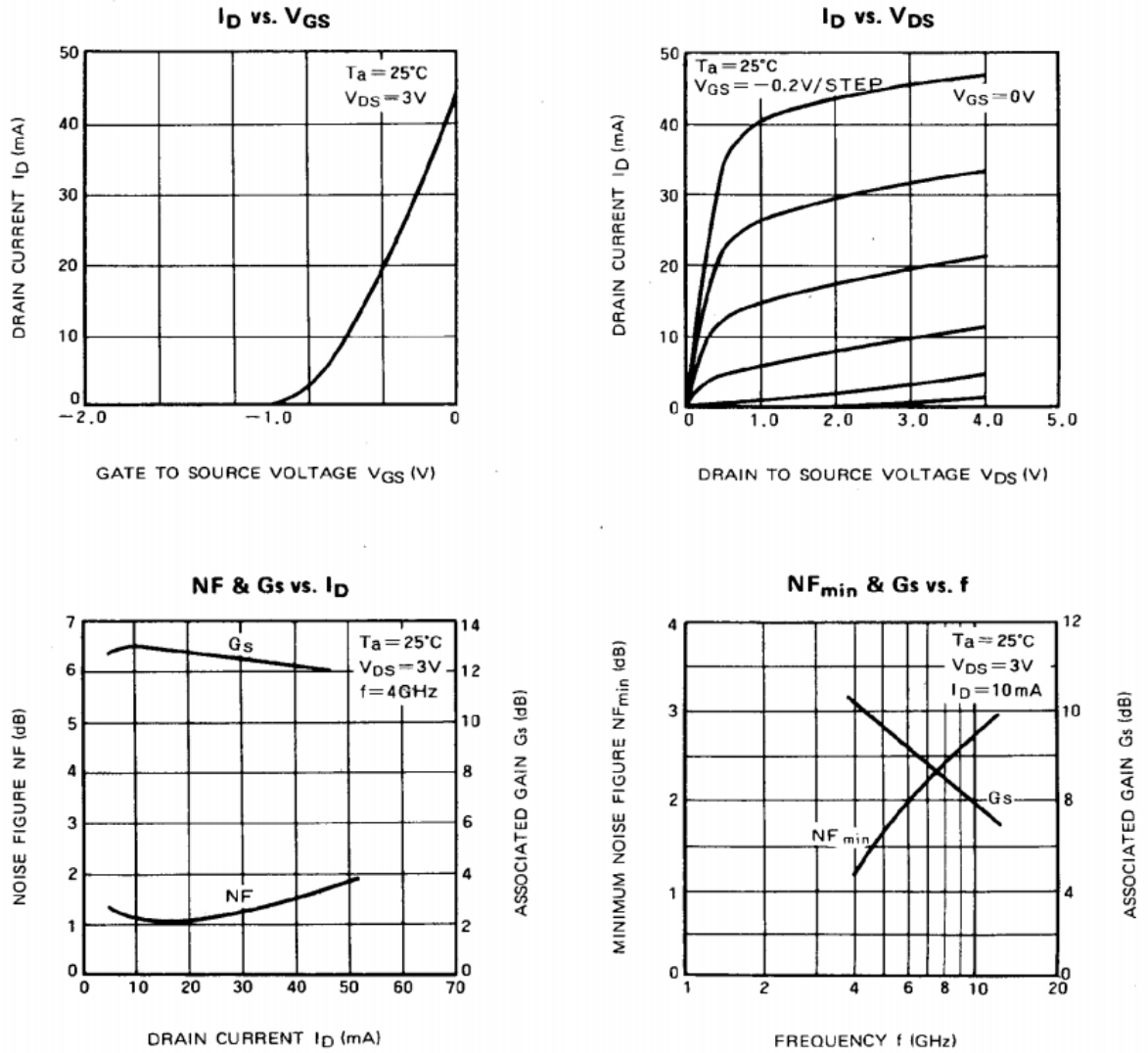

Figure 3.14: Typical characteristics of MGF1302 from datasheet.

The HEMT footprint was designed in KiCad with the specified dimensions in the datasheet and then soldered to the output PCB using a CHIPQUIK solder paste followed by heating in oven at 150° C for firm soldering.

3.4.2 Connectors

All the connections were made using Rosenberger Mini-SMP connectors. Rosenberger Mini-SMP connectors are extremely small coaxial connectors, approximately 70 % of standard SMP size. They are designed for applications up to 65 GHz and mainly for high-speed signal transmission (typically 10 or 40 Gbps). Plugs are available as smooth bore-versions – for plug-in technology and backplane applications – and as vibration resistant full detent types, for the highest mechanical loads. Surface-mount technology allows for excellent transmission characteristics as well as automated installation, thanks to the unique tape and reel packaging. In addition to small Board-to-Board distances, equalisation of radial and axial misalignments, different holding forces, and a quick and cost-effective assembly design are all important features. Surface mount link quality is influenced by a number of factors, including substrate thickness and board stack-up. Surface mount link quality is influenced by a number of factors, including substrate thickness and board stack-up. We have used 18S101-40ML5 straight plug and 18S243-40ML5 right angle plug.

Figure 3.15: 18S101-40ML5

Figure 3.16: 18S243-40ML5

3.4.3 Load Resistor (R_L)

R_L is used to bias the HEMT drain with the voltage V_{dd}. R_L must be greater than the cable resistance to ensure stable operation. As a result, we select $R_L = 1$ kΩ. When the HEMT's drain-source resistance is roughly equal to R_L, the maximum amplification is predicted. To reduce the output circuit's heat load, we have placed R_L at room temperature (RT) and external to the output PCB.

3.5   PCB Footprints

The output PCB was commercially printed with high resolution due to the nature of dimensions of the HEMT. The footprints necessary for generating gerber files and drill files were made using KiCad. The footprints included those of the HEMT and mini-smp connectors.
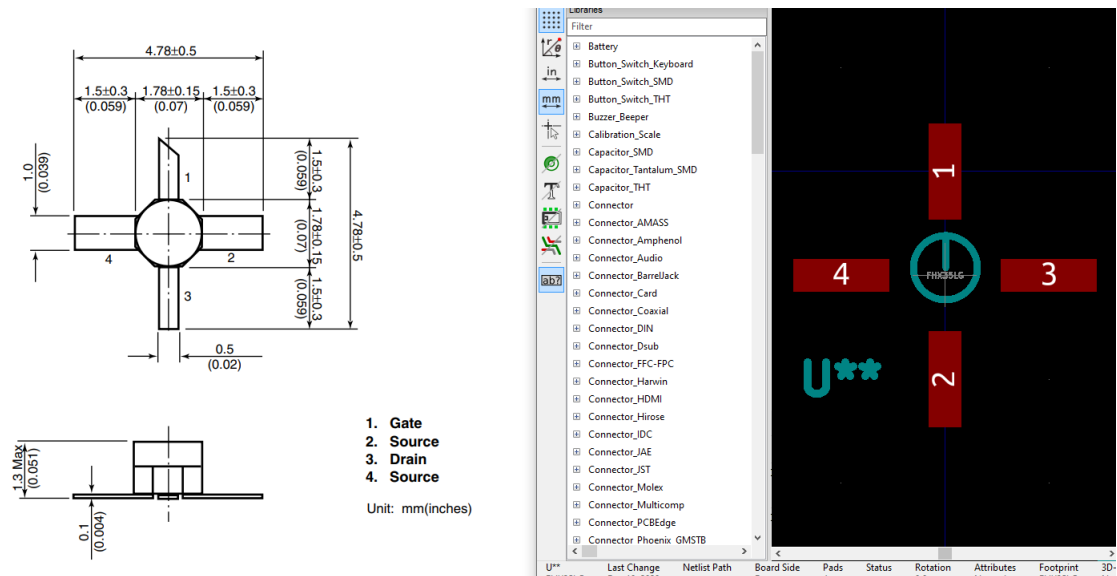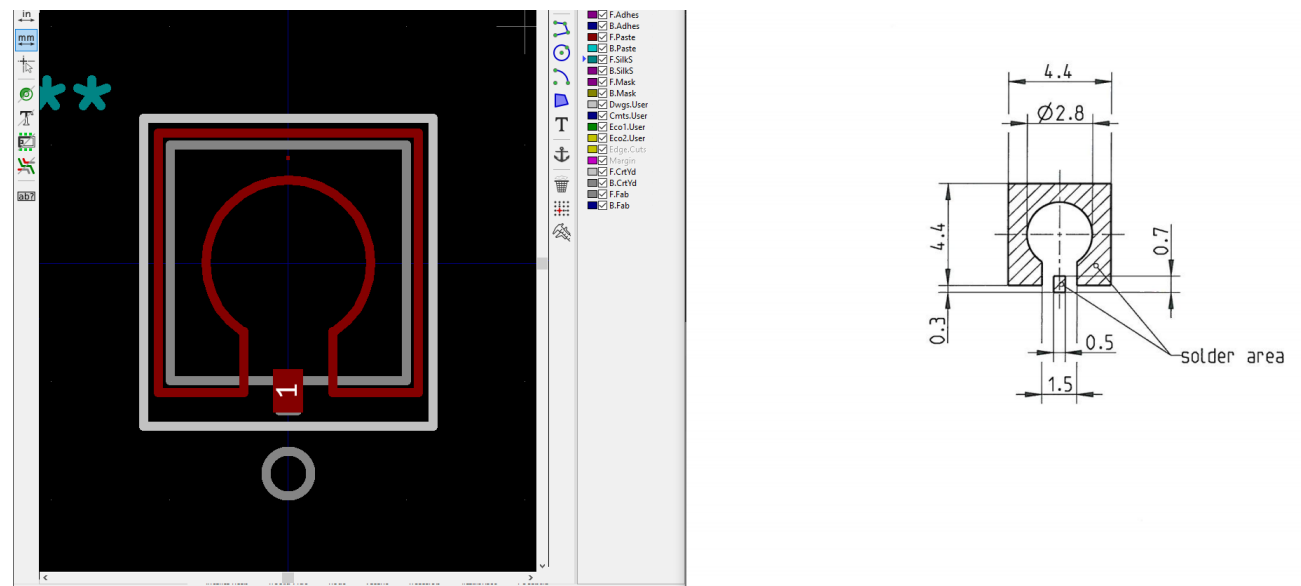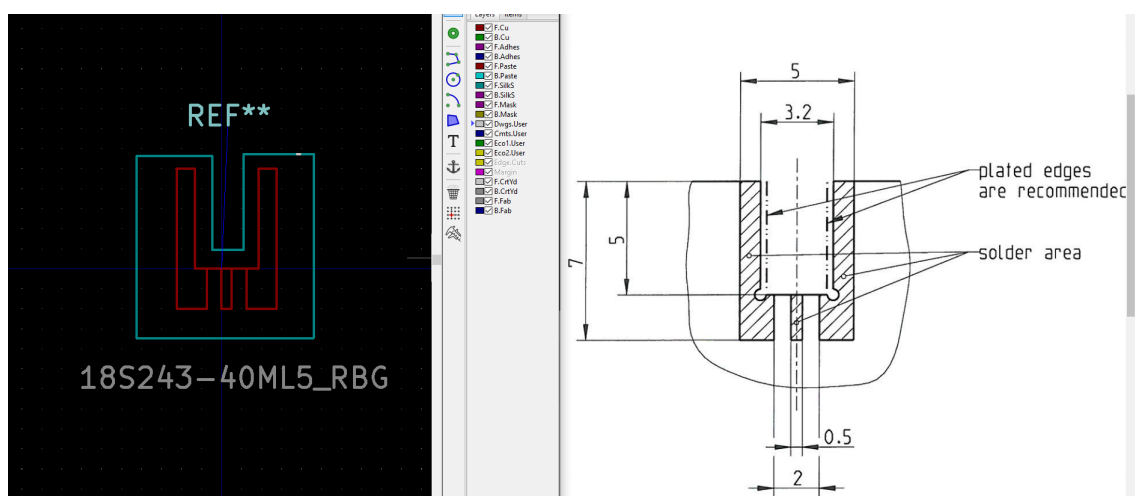

Figure 3.17: MGF1302

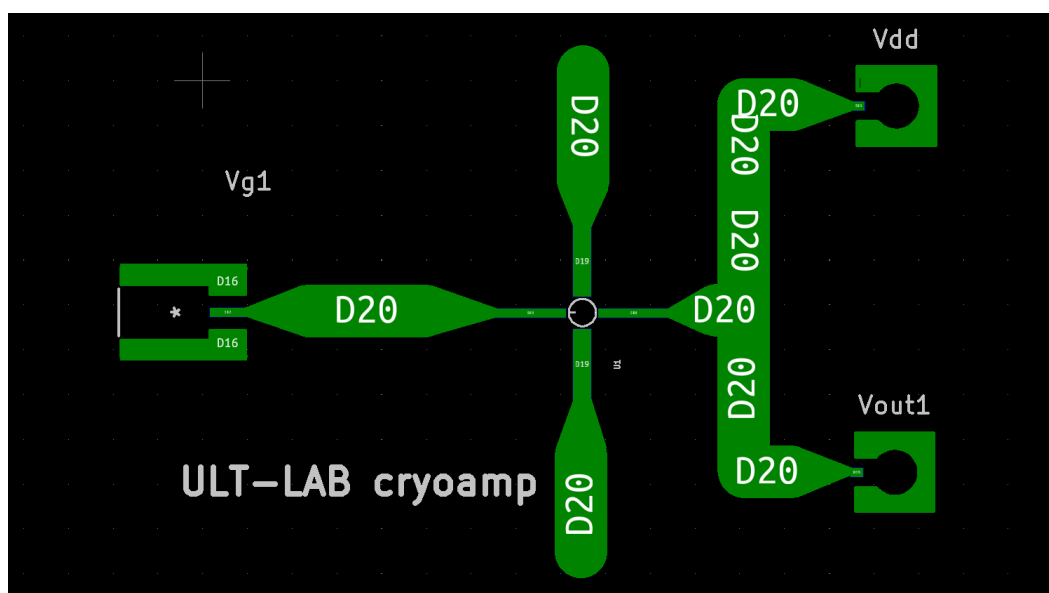Figure 3.18: 18S101-40ML5.

Figure 3.19: 18S243-40ML5

Figure 3.20: Output PCB.

Chapter 4

Progress and Results

We designed and constructed an integrated impedance bridge that operates from room temperature down to cryogenic temperatures. The input circuit, bridge circuit and output circuit have been fabricated. We will test the set-up with varactor diode and then move on to graphene sample. The DUT PCB was fabricated using photolithography technique and the bridge PCB was first designed using KiCad and then it was commercially printed for higher precision from the generated gerber and drill files. We optimised this process of photolithography and the etching process for fabricating microstrips on FR4 substrate. All the connections were made using mini-smp connectors which were soldered to the PCB using solder paste followed by heating in the oven. All the connections were checked with the help of a multimeter for any possible short circuiting. The connectoins of the input circuit were made using metal soldering. The HEMT was also checked using a load resistor for output characteristics. We have also checked and demonstrated the addition AC and DC signals using an audio transformer.
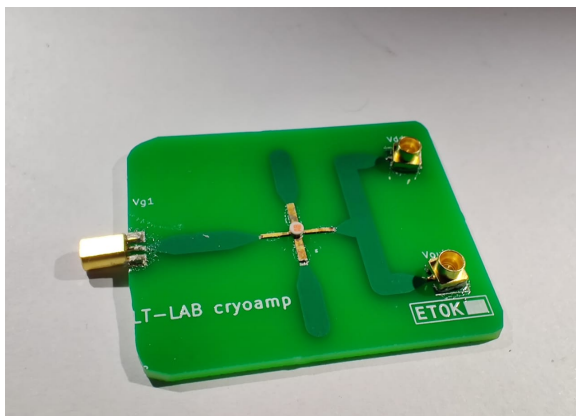

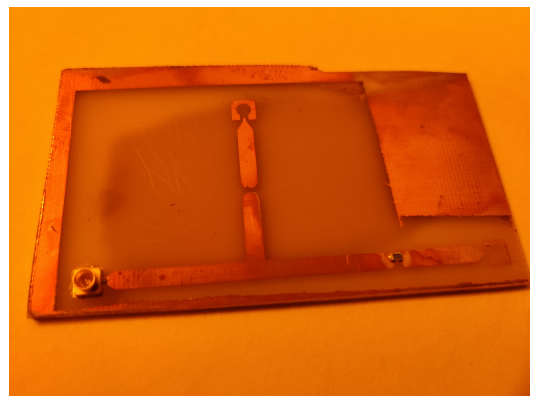Figure 4.1: Bridge circuit PCB

Figure 4.2: DUT PCB

The optimisation of photolithography process led to the fabrication of accurate microstrip design for the DUT PCB. We checked the working of AC-DC summer by applying AC voltage across pin 1 and 3 with the help of an oscilloscope and then giving constant DC source across pin 4 and 6 and measuring the output from pin 5 of the audio transformer.
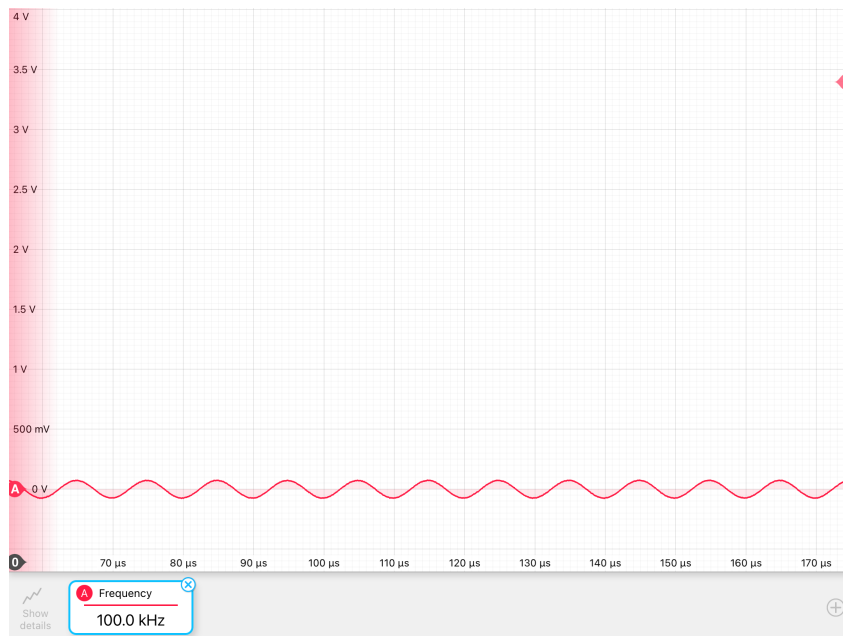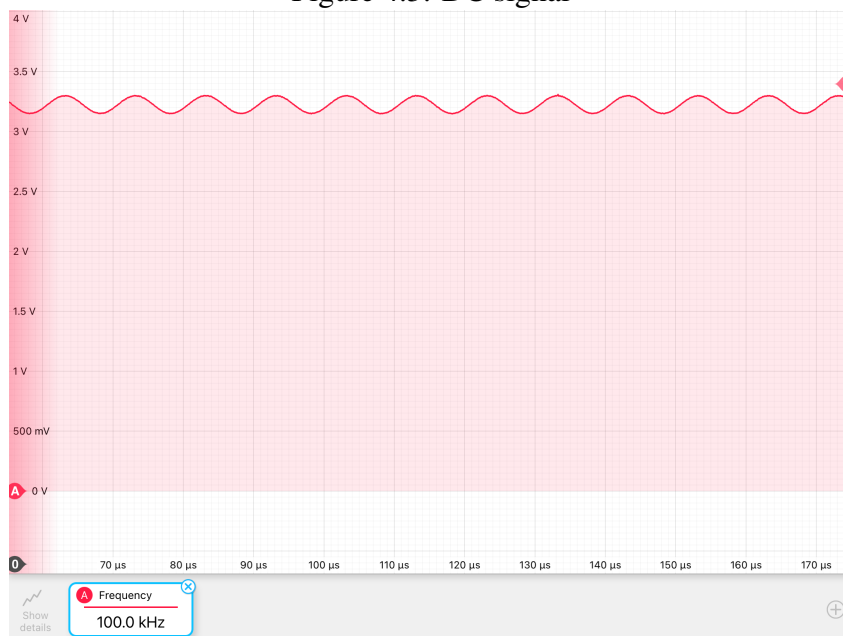

Figure 4.3: DC signal

Figure 4.4: AC + DC signal

We were successfully able to add AC and DC signals with the help of an triad magnetics audio transformer which acts as the input circuit of our set-up.

We checked the working of the HEMT by measuring its out put charecteristics where measuring the drain current with the drain-source voltage when no bias is applied. The load resistor was 1 kΩ. The DC voltage was applied using Agilent single output DC supply.
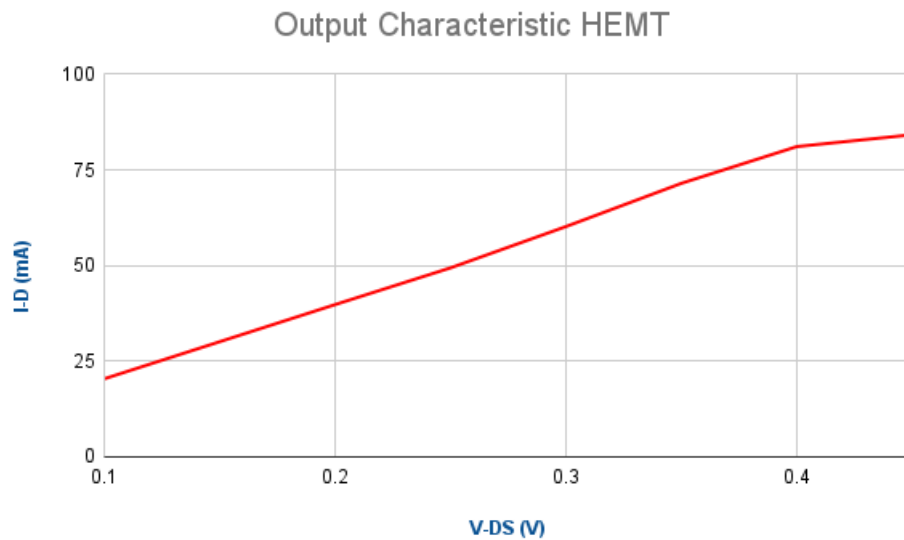

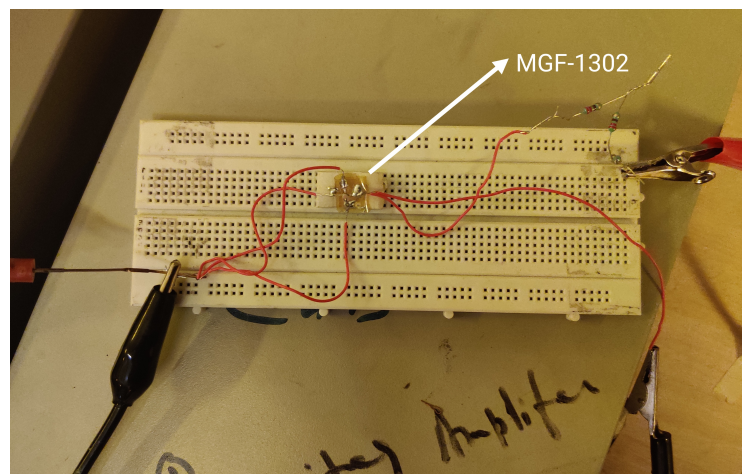Figure 4.5: output characteristics of MGF1302

Figure 4.6: Circuit for measuring output characteristics.

The set-up is ready and measurements to find out the resolution of capacitance will be done after characterisation of the HEMT at low temperatures as explained in the bridge operation. Further we will be using graphene as a sample for low temperature and magnetic field dependent measurements.

Appendix A

Vortex mixer machine for etching.

We have optimised the photolithography process, etching the PCB being a crucial step. The etching process requires mixing and disturbing the solution of FeCl_3 with the PCB inside it. This process takes approximately 30 minutes and more depending on the size of the PCB. Hence we made a homemade vortex mixer machine to carryout this process. The circuit for
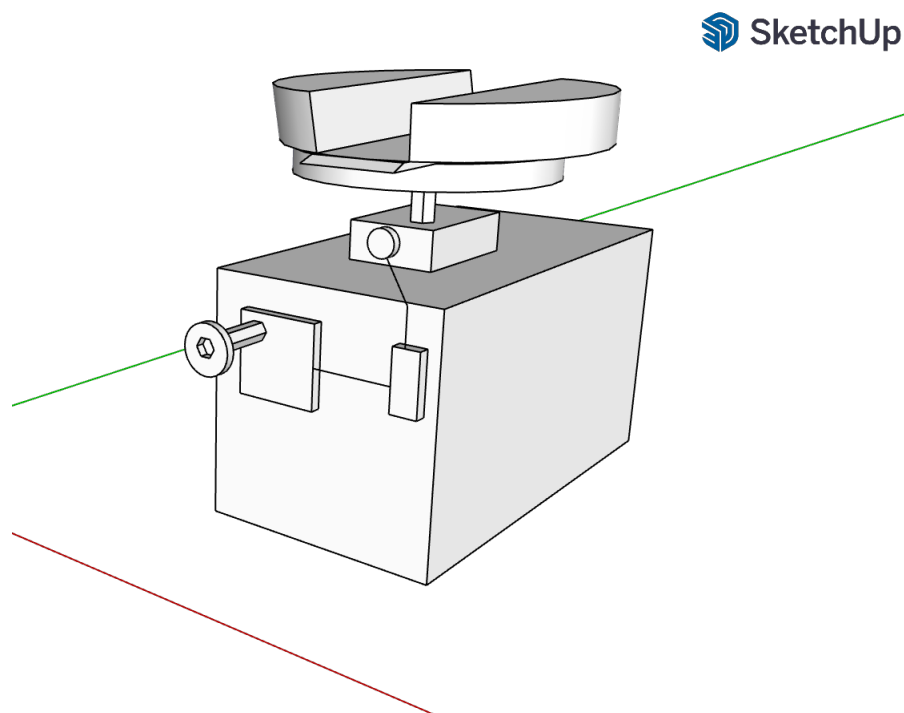

Figure A.1: CAD design of the vortex mixer.

this constitutes of a voltage regulator made earlier, a motor and a switch. The purpose of the voltage regulator is to act as a speed regulator to control the rotations per minute as to speed up the etching process.

This is a temporary structure, we will be developing a stable solid outer frame and will put the circuit inside of the device. The power source for it is a battery now which we will be replacing by an adaptor for a more permanent structure.

Figure A.2: constructed vortex mixer for etching

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